

### REMARKS

Claims 1, 15, 17-18, 20 and 29 are amended. Claims 13-14 and 33-36 are canceled. New claims 37-40 are added. No new matter is added as the originally-filed application supports the new claims at, for example, page 10 and Fig. 6. Claims 1-12, 15-20, 29-32 and 37-40 are pending in the application.

Claims 1-12, 15-20 and 29-32 stand rejected under 35 USC §103(a) as being unpatentable over Ku et al. ("The Application of Ion-Beam Mixing, Doped Silicide, and Rapid Thermal Processing to Self-Aligned Silicide Technology", VLSI Technology, Systems and Applications, May 17-19, 1989, pages 337-341), or Chen et al. (US Patent No. 5,472,896).

Regarding the rejection of claim 1 based on Ku and Chen, such claim is amended to recite after providing a conductivity-enhancing impurity [within a silicide], etching a polysilicon layer and the silicide layer into a conductive line shape. No new matter is added as the originally-filed application supports such amendment language at, for example, pages 9-10 and Fig. 6. Ku teaches after patterning a layer of titanium over a patterned polysilicon gate, annealing to form a silicide (page 337, first col., last paragraph to second col., first paragraph; Fig. 1). After annealing, implanting impurity ions into the silicide layer (page 337, first col., last paragraph to second col., first paragraph; Fig. 1). Chen teaches forming a tungsten silicide layer 16 over a polysilicon layer 14 and patterning the layers **before** an ion implantation step (col. 4, Ins. 29-44; Figs. 3b-e; and col. 5, Ins. 1-20; Figs. 4b-e). Consequently, the art of record, singularly

or in any combination, teaches the polysilicon and silicide layers are patterned **b fore** the implanting of the impurity ions. Accordingly, in no fair or reasonable interpretation does Ku and Chen, singularly or in any combination, teach or suggest **after providing** a conductivity-enhancing impurity [within a silicide], etching a polysilicon layer and the silicide layer into a conductive line shape as recited in claim 1. Since Ku and Chen, singularly or in any combination, fail to teach or suggest a positively recited limitation of claim 1, claim 1 is allowable. Applicant respectfully requests allowance of claim 1 in the next Office Action.

Claims 2-12 and 37 depend from independent claim 1, and therefore, are allowable for the reasons discussed above with respect to the independent claim, as well as for their own recited features which are not taught or shown by the art of record.

Regarding the obviousness rejections against claim 15 based on Ku and Chen, such claim is amended to recite during forming of a silicide layer, providing a conductivity-enhancing impurity within the silicide layer. No new matter is added as the originally-filed application supports such amendment language at, for example, pages 9-10 and Fig. 6. Ku teaches implanting impurity ions into a silicide layer **after** forming the silicide layer (page 337, first col., last paragraph to second col., first paragraph; Fig. 1). Chen teaches implanting impurity ions into a silicide layer **after** forming the silicide layer (col. 4, Ins. 29-44; Figs. 3b-e; and col. 5, Ins. 1-20; Figs. 4b-e). Accordingly, Ku and Chen, singularly or in any combination, fail to teach or suggest during forming of a silicide layer, providing a conductivity-enhancing impurity within the silicide layer as

recited in claim 15. Since Ku and Chen, singularly or in any combination, fail to teach or suggest a positively recited limitation of claim 15, such claim is allowable. Applicant respectfully requests allowance of claim 15 in the next Office Action.

Claims 16-19 and 38 depend from independent claim 15, and therefore, are allowable for the reasons discussed above with respect to the independent claim, as well as for their own recited features which are not taught or shown by the art of record.

Regarding the obviousness rejections against claim 20 based on Ku and Chen, such claim is amended to recite subjecting a silicide layer to a rapid thermal processing step to exceed 850°C for at least 10 seconds while exposing the silicide layer to a oxygen-comprising atmosphere. No new matter is added as the originally-filed application supports such amendment language at, for example, page 8. Ku teaches a rapid thermal processing step exposing a silicide layer to an NH<sub>3</sub> or N<sub>2</sub> atmosphere, but **not** an oxygen-comprising atmosphere as recited in claim 20 (page 337, second paragraph, col. 2, third paragraph; page 338, col. 2, last paragraph; Fig. 6). Chen does not teach a rapid thermal processing step, and an electronic search of the reference verifies the same. Accordingly, Ku and Chen, singularly or in any combination, fail to teach or suggest subjecting a silicide layer to a rapid thermal processing step to exceed 850°C for at least 10 seconds while exposing the silicide layer to a oxygen-comprising atmosphere as recited in claim 20. Since Ku and Chen, singularly or in any combination, fail to teach or suggest a positively recited limitation of claim 20, such claim is allowable. Applicant respectfully requests allowance of claim 20 in the next

Office Action.

Claim 39 depends from independent claim 20, and therefore, is allowable for the reasons discussed above with respect to the independent claim, as well as for its own recited features which are not taught or shown by the art of record.

Regarding the obviousness rejections against claim 29 based on Ku and Chen, such claim is amended to recite sputter depositing a silicide layer. No new matter is added as the originally-filed application supports such amendment language at, for example, pages 9-10. Ku does not teach sputter depositing. Chen does not teach sputter depositing. Accordingly, Ku and Chen, singularly or in any combination, fail to teach or suggest sputter depositing a silicide layer as recited in claim 29. Since Ku and Chen, singularly or in any combination, fail to teach or suggest a positively recited limitation of claim 29, such claim is allowable. Applicant respectfully requests allowance of claim 29 in the next Office Action.

Claims 30-32 and 40 depend from independent claim 29, and therefore, are allowable for the reasons discussed above with respect to the independent claim, as well as for their own recited features which are not taught or shown by the art of record.

Further, Applicant herewith submits a duplicate copies of the Information Disclosure Statement, Supplemental Information Disclosure Statements and Form PTO-1449s filed together in this application on June 11, 1999, February 7, 2002, March 13, 2002, and May 6, 2002. **No initialed copies of the PTO-1449s have been received back from the Examiner.** To the extent that the submitted references listed


Appl. No. 09/332,271

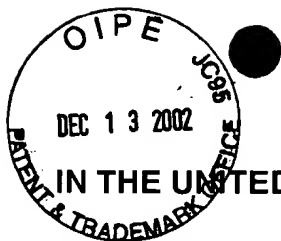
on the Form PTO-1449s have not already been considered, and the Form PTO-1449s have not been initialed with copies being returned to Applicant, such examination and initialing is requested at this time, as well as return of the initialed Form PTO-1449s to the undersigned.

This application is now believed to be in immediate condition for allowance, and action to that end is respectfully requested. If the Examiner's next anticipated action is to be anything other than a Notice of Allowance, the undersigned respectfully requests a telephone interview prior to issuance of any such subsequent action.

Respectfully submitted,

Dated: 12-13-02

By:   
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Reg. No. 40,045



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. .... 09/332,271  
Filing Date ..... June 11, 1999  
Inventor ..... Klaus Florian Schuegraf et al.  
Assignee ..... Micron Technology, Inc.  
Group Art Unit ..... 2812  
Examiner ..... Ron E. Pompey  
Attorney's Docket No. .... MI22-532  
Title: Methods for Forming Wordlines, Transistor Gates, and Conductive  
Interconnects, and Wordline, Transistor Gate, and Conductive Interconnect  
Structures

**VERSION WITH MARKINGS TO SHOW CHANGES MADE ACCOMPANYING  
RESPONSE TO AUGUST 13, 2002 FINAL OFFICE ACTION**

**In the Claims**

The claims have been amended as follows. Underlines indicate insertions and  
~~strikeouts~~ indicate deletions.

1. (Amended) A method of forming a conductive line comprising the following  
steps:

forming a polysilicon layer;

forming a silicide layer against the polysilicon layer;

providing a conductivity-enhancing impurity within the silicide layer; and

after the providing of the conductivity-enhancing impurity, providing etching the  
polysilicon layer and the silicide layer into a conductive line shape.

Claims 13-14 have been canceled.

15. (Amended) A method of forming a conductive line comprising the following steps:

forming a polysilicon layer;

forming a silicide layer against the layer of polysilicon;

during the forming of the silicide layer, providing a conductivity-enhancing impurity within the silicide layer; and

after providing the conductivity-enhancing impurity within the silicide layer, subjecting the silicide layer to a processing step of over 850°C for at least 10 seconds.

17. (Amended) The method of claim 15 wherein the forming the silicide layer comprises depositing a metal layer over the polysilicon and reacting the metal layer with the polysilicon, and wherein the conductivity-enhancing impurity is provided ~~within the metal layer after the reacting the metal layer with the polysilicon~~ during a CVD process.

18. (Amended) The method of claim 15 wherein the conductivity-enhancing impurity is ~~implanted into the silicide layer~~ provided during one of a CVD process and a sputter deposition.

20. (Amended) A method of forming a conductive line comprising the following steps:

forming a polysilicon layer;

forming a silicide layer against the layer of polysilicon;

providing a conductivity-enhancing impurity within the silicide layer; and

subjecting the silicide layer to a rapid thermal processing step ~~of over~~ to exceed 850°C for at least 10 seconds while exposing the silicide layer to an oxygen-comprising atmosphere.

29. (Amended) A method of forming a conductive line comprising:

forming a polysilicon layer;

~~forming~~ sputter depositing a silicide layer over and proximately adjacent only the polysilicon layer; and

providing a conductivity-enhancing impurity within the silicide layer.

Claims 33-36 are canceled.

**-END OF DOCUMENT-**